ABSTRACT

A CMOS device structure, and a method of fabricating the CMOS device, featuring a gate insulator layer comprised of a high k metal oxide layer, has been developed. The process features formation of recessed, heavily doped source/drain regions, and of vertical, polysilicon LDD spacers, prior to deposition of the high k metal oxide layer. Removal of a silicon nitride shape, previously used as a mask for definition of the recessed regions, which in turn are used for accommodation of the heavily doped source/drain regions, provides the space to be occupied by the high k metal oxide layer. The integrity of the high k, gate insulator layer, butted by the vertical polysilicon spacers, and overlying a channel region provided by the non-recessed portion of the semiconductor substrate, is preserved via delayed deposition of the metal oxide layer, performed after high temperature anneals such as the activation anneal for heavily doped source/drain regions, as well as the anneal used for metal silicide formation.